

What is claimed is;

1. An image processing apparatus comprising at least two signal processor modules interconnected each other in series, each of the signal processor modules having an input port through which data is input, a memory which stores data, a signal processor portion which carries out processing on input data according to program and an output port through which data is output, wherein the improvement comprises that

at least one of the signal processor modules outputs both unprocessed input data and processed data obtained by processing the input data.

2. An image processing apparatus as defined in Claim 1 in which

said at least one of the signal processor modules stores within one cycle in the memory unprocessed input data as input through the input port and processed data obtained by reading out and processing unprocessed input data stored in the memory predetermined number of cycles before and outputs within one cycle through the output port unprocessed data and processed data stored in the memory predetermined number of cycles before, and

the other signal processor module(s) stores within one cycle in the memory unprocessed input data as input through the input port and processed data obtained by reading out and processing unprocessed input data stored in the memory predetermined number of cycles before and outputs within one

cycle through the output port processed data stored in the memory
predetermined number of cycles before, or stores in the memory
unprocessed input data as input through the input port and
outputs through the output port unprocessed input data stored
5 in the memory predetermined number of cycles before.

3. An image processing apparatus as defined in Claim
2 further comprising a synchronous circuit which causes data
transfer between signal processor modules to occur in
synchronization with clocks which are the same in phase and
10 frequency.

4. An image processing apparatus as defined in Claim
3 in which the data transfer widths between the signal processor
modules are equal to each other and the synchronous circuit
determines the frequency of the transfer clock on the basis
15 of the data transfer rate between the pair of signal processor
modules between which the largest amount of data is to be
transferred.

5. An image processing apparatus as defined in Claim
1 in which Further, a mounting means on which a signal processor
20 module is removably mounted is provided for at least one of
the signal processor modules and a switching means is provided
for said at least one signal processor module to transfer data
to the signal processor module through its input port when it
is mounted on the mounting means and to transfer the same to
25 a component rearward of the signal processor module when it
is not mounted on the mounting means.